Amendments to the Specification

Please replace the BRIEF DESCRIPTION OF THE DRAWINGS with the following list:

FIG. 1 shows how a group of capacitors can be connected to provide a wide range of capacitances.

FIGs. 2a and 2b shows ~~the starting point~~ initial steps for the process of the present invention.

FIGs. 3 and 4 shows how several micro-capacitors may be formed without using up too much chip real estate.

FIG. 5 shows how connections are made to the individual capacitors.

FIG. 6 shows the circuit of FIG. 1 modified to produce a specific capacitance value.

FIG. 7 illustrates the addition of external contacts.

FIG. 8 shows how the invention may be adapted to provide a field programmable capacitor.

Please replace the first paragraph on page 5 with the following amended paragraph:

Referring now to FIG. 2a, the process of the present invention begins with the provision of suitable substrate 21 on which is already present (or is to be added) an electrical circuit of some kind including contact pads, such as 26, to which a capacitor is to be connected. Most commonly, though not necessarily exclusively, this will be the topmost layer of an integrated circuit on a silicon wafer.

Please replace the first paragraph on page 6 with the following amended paragraph:

After deposition of a barrier layer (not shown) in via hole 27 it is overfilled with tungsten and then planarized so as to remove all tungsten not inside via 27, resulting in the formation of tungsten via 35 (FIG. [3] 2b). Then, as seen in FIG. 2b, three trenches

24, that extend through layer 23 as far as etch stop layer 25, are etched. The presence of layer 25 ensures that all trenches have exactly the same depth. Each trench has a width between about 0.1 and 0.8 microns and the trenches are separated from one another by between about 0.1 and 1 microns, depending on technology design rules.

Please replace the first paragraph on page 7 with the following amended paragraph:

We refer now to FIG. 4. Metal layer 15 is deposited on high dielectric constant layer 32 and then patterned to form four unconnected top electrodes 151, 152, and [155] 153, all of whom are overlapped by common electrode 11. These correspond to the four capacitors marked 1, 1, 2, and 5 shown schematically in FIG. 1 so their relative areas are arranged to be in the ratio 1:1:2:5. Materials and thicknesses for layer 15 are similar to what was used for layer 11.

Please replace the second paragraph on page 7 with the following amended paragraph

Referring next to FIG. 5, top dielectric layer 53 is then deposited on layer 15 (as well as any exposed parts of layer 32) and four via holes 16 are etched through layer [23] 53 so as to expose contact area for each of top electrodes 151, 152, and [155] 153. Via holes 16 are then filled with tungsten as already described above so as to provide contacts such as 54 for connection to the capacitor top plates.

Please replace the fourth paragraph on page 7 with the following amended paragraph (please note that the underlined phrases were already underlined in the original text and do not represent added material):

In a first embodiment a metal layer (not shown) is laid down on layer [23] 53 and then patterned to make permanent (hard-wired) connections to electrode [155] 153 and either of the electrodes 151. In a second embodiment, a contact wire (not shown) is provided near each contact, such as 54, and then connected to it through a field programmable device. This results in a field programmable capacitor whose value can be adjusted at the time that it is needed in the field. Examples of possible field programmable devices include fusible links, anti-fuses, resistors, capacitors, and pass transistors.

Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1-15 Canceled.

16.(currently amended) An adjustable capacitor, comprising:

a silicon wafer having a topmost layer on which are contact pads connected to a circuit contained in said wafer;

a base dielectric layer on said topmost layer and said contact pads;

an etch stop layer on said base dielectric layer;

a support dielectric layer on said etch stop layer;

a tungsten via, extending through said support dielectric layer, said etch stop layer, and said base dielectric layer, and contacting said contact pad;

three trenches that extend through said support dielectric layer as far as said etch stop layer;

a common capacitor electrode on said support dielectric layer, including inside said trenches, that contacts said tungsten via;

on said common capacitor electrode, a layer of high dielectric constant material that fully overlaps said common capacitor electrode;

on said high dielectric constant layer, four unconnected top electrodes, all of whom are overlapped by said common electrode, said top electrodes having, relative to one another, areas in the ratio 5:2:1:1;

a top dielectric layer on said top electrodes and said high dielectric constant

layer;

four tungsten vias, extending through said top dielectric layer, that contact each top electrode, one such via per electrode; and

on said top dielectric layer, permanent electrical connections between said top electrodes, whereby said adjustable capacitor has a specific capacitance value.

17.(original) The capacitor described in claim 16 wherein said base dielectric layer is selected from the group consisting of silicon oxide, black diamond, and all dielectrics having a dielectric constant less than about 5 and said base dielectric layer is deposited to a thickness between about 200 and 5,000 Angstroms.

18.(original) The capacitor described in claim 16 wherein said etch stop layer is selected from the group consisting of silicon nitride and silicon carbide and is deposited to a thickness between about 20 and 500 microns.

19.(original) The capacitor described in claim 16 wherein said support dielectric layer is selected from the group consisting of silicon oxide, black diamond, and all dielectrics having a dielectric constant less than about 5 and said support dielectric layer is deposited to a thickness between about 200 and 5,000 Angstroms.

20.(original) The capacitor described in claim 16 wherein said common capacitor electrode and said top electrodes are a metal selected from the group consisting of Al, AlCu, Cu, Ti, TiN, and Ta and have a thickness between about 200 and 5,000 Angstroms.

21.(original) The capacitor described in claim 16 wherein said layer of high dielectric constant material is selected from the group consisting of silicon nitride, tantalum oxide,

aluminum oxide, and hafnium oxide and is deposited to a thickness between about 20 and 500 Angstroms.

22.(original) The capacitor described in claim 16 wherein each trench has a width between about 0.1 and 0.8 microns and said trenches are separated from one another by between about 0.1 and 0.8 microns.

23.(currently amended) A field programmable capacitor, comprising:

a silicon wafer having a topmost layer on which are contact pads connected to a circuit contained in said wafer;

a base dielectric layer on said topmost layer and said contact pads;

an etch stop layer on said base dielectric layer;

a support dielectric layer on said etch stop layer;

a tungsten via, extending through said support dielectric layer, said etch stop layer, and said base dielectric layer, and contacting said contact pad;

three trenches that extend through said support dielectric layer as far as said etch stop layer;

a common capacitor electrode on said support dielectric layer, including inside said trenches, that contacts said tungsten via;

on said common capacitor electrode, a layer of high dielectric constant material that fully overlaps said common capacitor electrode;

on said high dielectric constant layer, four unconnected top electrodes, all of whom are overlapped by said common electrode, said top electrodes having, relative to one another, areas in the ratio 5:2:1:1;

a top dielectric layer on said top electrodes and said high dielectric constant layer;

four tungsten vias, extending through said top dielectric layer, that contact each

top electrode, one such via per electrode; and

on said top dielectric layer, a metallic contact wire for each of said four ~~filled~~ tungsten vias ~~holes~~, said contact wires being connectable to each other through field programmable devices.

24.(original) The capacitor described in claim 23 wherein said field programmable devices are selected from the group consisting of fusible links, anti-fuses, and pass transistors.

25.(original) The capacitor described in claim 23 wherein said base dielectric layer is selected from the group consisting of silicon oxide, black diamond, and all dielectrics having a dielectric constant less than about 5 and said base dielectric layer is deposited to a thickness between about 200 and 5,000 Angstroms.

26.(original) The capacitor described in claim 23 wherein said etch stop layer is selected from the group consisting of silicon nitride and silicon carbide and is deposited to a thickness between about 20 and 500 microns.

27.(original) The capacitor described in claim 23 wherein said support dielectric layer is selected from the group consisting of silicon oxide, black diamond, and all dielectrics having a dielectric constant less than about 5 and said support dielectric layer is deposited to a thickness between about 200 and 5,000 Angstroms.

28.(original) The capacitor described in claim 23 wherein said common capacitor electrode and said top electrodes are a metal selected from the group consisting of Al, AlCu, Cu, Ti, TiN, and Ta and have a thickness between about 200 and 5,000 Angstroms.

29.(original) The capacitor described in claim 23 wherein said layer of high dielectric constant material is selected from the group consisting of silicon nitride, tantalum oxide, aluminum oxide, and hafnium oxide and is deposited to a thickness between about 20 and 500 Angstroms.

30.(original) The capacitor described in claim 23 wherein each trench has a width between about 0.1 and 0.8 microns and said trenches are separated from one another by between about 0.1 and 0.8 microns.